REMARKS

Claims 1-10, 12-21 and 23 are pending.

Claims 11 and 22 have been cancelled without prejudice or disclaimer of the subject matter recited therein.

Claims 1, 5, 6, 12, 16 and 17 are being amended. No new matter is being added. Basis for the amendments to Claims 1 and 12 can most easily be seen from FIG. 3 where the output stage can be seen within the box defined by the broken line identified as reference numeral 320. The terms "direct current (DC)" have been deleted from these claims. Additionally, reference to first control loop means and second control loop means have been amended to "control loop means" and "output loop means". Basis for the term "output loop" in Claim 1 can be found on page 9, line 7, of the description. Since the term "main loop" has been generalized to "control loop means" it is submitted that the skilled person would also implicitly understand that the term "output loop" can be generalized as "output loop means".

The phrase "may be obtained with a lower load" has been clarified due to the use of the conditional tense in these respective parts of Claims 1 and 12. Consequently, the wording "the output loop means providing the low output impedance for coupling across the load so as to provide" has been employed instead. Basis for this amendment can be found on: page 6, line 29 – page 7, line 3; page 8, line 15 – page 9, line 2; and page 9, lines 13-24. The recitation in the final two lines of Claims 1 and 12 relating to lowering of the capacitance of the load can be directly and unambiguously derived from page 8, lines 15-22.

In section 2 of the Office Action, Claims 1-23 are rejected under 35 USC § 102(a) as being anticipated by US Patent No. 6,300,749 (hereinafter referred to as the "Castelli et al. patent"). Applicants are traversing this rejection.

The application includes two independent claims, namely Claims 1 and 12. Below, Applicants explain that the Castelli et al. patent does not disclose all of the elements of Claims 1 and 12 as amended.

The Castelli et al. patent relates to a method and apparatus of dynamically modifying internal compensation of a low drop-out linear voltage regulator. As explained in col. 1, lines 45-57, traditional low drop-out voltage regulators have an output dominant pole that is determined by an output capacitance (Co). This pole is movable according to load variations. Col. 2, lines 3-13 explain that a circuit component is always provided to introduce a zero to compensate for the effects of the output pole mentioned above. It is further explained that the compensation is critical due to the need to guarantee regulator stability. Referring to FIG. 3 of the Castelli et al. patent and col. 4, lines 9-29, the buffer stage 4 de-couples the gain stage 3 from the PMOS transistor 8 so that a compensation of the entire LDO regulator can be implemented by means of a delay phase network. The delay phase network is, in this example, formed by an RC network 10 disposed between the gain stage 3 and the buffer stage 4. The delay stage network introduces a zero and a pole at a lower frequency. Further, the compensation zero is used to compensate for the effect of a second pole in the loop gain. The above-described implementation is the basis for subsequent embodiments described in the Castelli et al. patent. In this respect, FIG. 6 introduces a sensing transistor. However, the principal of operation is largely the same as in respect of the embodiment of FIG. 3. In this respect, stability is provided by creating a moving "zero".

Claim 1 recites a transistor means having an output stage for coupling to a load, the transistor means further comprising output loop means, the output loop means providing a low output impedance for coupling across the load so as to provide stability of operation by lowering a capacitance of the load.

The Castelli et al. patent does not teach the provision of transistor means comprising output loop means that provides a low output impedance for coupling across the load so as to provide stability of operation by lowering a capacitance of the load as recited in Claim 1. In contrast, and as mentioned above, the Castelli et al. patent provides compensation by implementing a moving zero. The provision of a low impedance across the load serves to move the pole provided by the load (which can be variable) as opposed to generating a moving zero. Hence, it can be seen that stability is achieved in a different way.

In view of the reasoning provided above, Applicants submit that the Castelli et al. patent does not anticipate Claim 1.

Claims 2-10 and 23 depend from Claim 1. By virtue of this dependence, Claims 2-10 and 23 are also novel over the Castelli et al. patent.

Claim 12 provides for a method for low drop-out voltage regulation that corresponds to apparatus of Claim 1. As explained above in support of Claim 1, the Castelli et al. patent does not disclose the feature of transistor means comprising output loop means, where the output loop means provide a low output impedance for coupling across the load so as to provide stability of operation by lowering a capacitance of the load as recited in Claim 12.

In view of the reasoning provided above, Applicants submit that the Castelli et al. patent does not anticipate Claim 12.

Claims 13-21 depend from Claim 12. By virtue of this dependence, Claims 13-21 are also novel over the Castelli et al. patent.

The case is believed to be in condition for allowance and notice to such effect is respectfully requested. If there is any issue that may be resolved, the Examiner is respectfully requested to telephone the undersigned.

Respectfully submitted,

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